VTC Inc.
Value the Customer™

VM312

10-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

July, 1993

FEATURES

- High Performance:
  - Read mode gain = 150 V/V
  - Low input noise = 0.8nV/√Hz maximum
  - Input capacitance = 25 pF maximum
  - Write current range = 10 mA to 40 mA
  - Head inductance range = 200 nH to 3 µH
  - Head voltage swing = 7 Vp-p minimum
  - Write current rise time = 5 ns
- Low Power Dissipation
- Enhanced System Write-to-Read Recovery Time
- Power Supply Fault Protection
- Schottky Isolated Damping Resistor Standard
- Write Unsafe Detection
- +5V and +12V Power Supply Requirement
- Mirror Image Pinout Options Available
- Available in 4, 6, 8, 9 or 10-Channel Options
- Pin-compatible with SSI 32R512

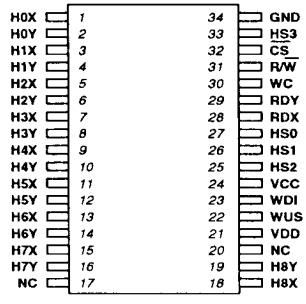
DESCRIPTION

The VM312 is a high-performance, low-power, bipolar monolithic read / write preamplifier designed for use with two-terminal thin-film recording heads. It provides write current control, data protection circuitry and a low-noise read preamplifier for ten channels. When unselected, the device enters a ***sleep mode***, with power dissipation reduced to less than 180mW. Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in the write mode.

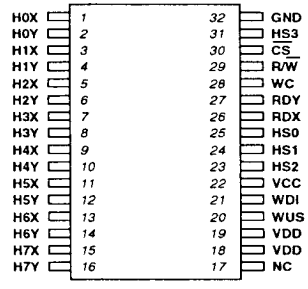
Very low power dissipation from +5V and +12V supplies is achieved through use of high-speed bipolar processing and innovative circuit design techniques. A 400-ohm damping resistor is included on-chip in series with a Schottky diode pair to maintain high input resistance in the read mode.

The VM312 is available in several different packages. Please consult VTC for package availability.

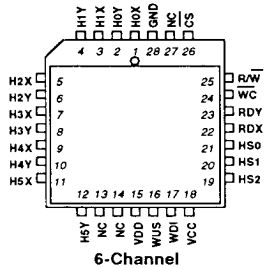
CONNECTION DIAGRAMS



9-Channel
34-lead SOIC



8-Channel
32-lead SOIC



6-Channel
28-lead PLCC

For additional connection diagrams see the last page of this data sheet.

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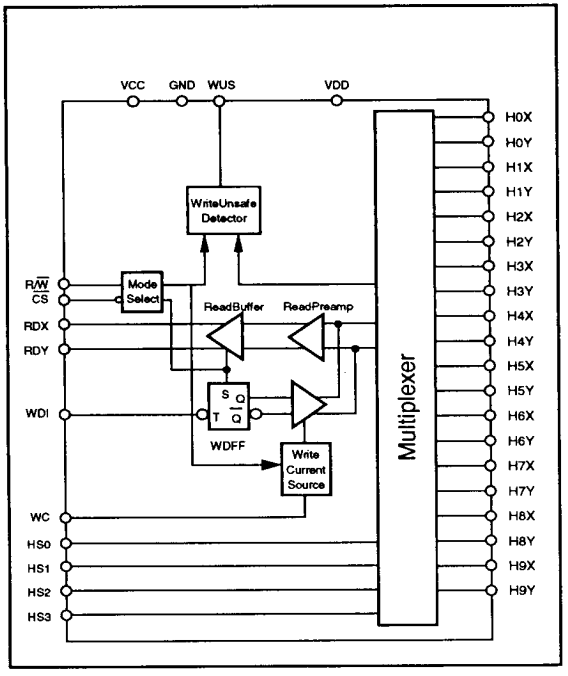
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +14V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{DD} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +14V

Output Current:
- RDX, RDY: I_O ..... -10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 28-lead SOIC ..... 65°C/W
- 32-lead SOIC ..... 55°C/W
- 34-lead SOIC ..... 60°C/W
- 44-lead SOIC ..... 55°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} ..... 12V ± 10%
- V_{CC} ..... 5V ± 10%

Operating Junction Temperature ..... 0°C to 125°C

CIRCUIT OPERATION

The VM312 addresses ten two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, CS and R/W, as shown in Tables 1 and 2. Internal resistor pullups provided on pins CS and R/W will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM312 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pin WDI (write data input).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 1.71V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 1.65\ V / R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM312H because the internal damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single R_{WC} resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, may be required to clear the WUS flag.

- No write current
- Open head
- Device not selected
- WDI frequency too low
- Device in read mode

Read Mode

Read mode configures the VM312 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When CS is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 180 mW for a ***sleep mode***.

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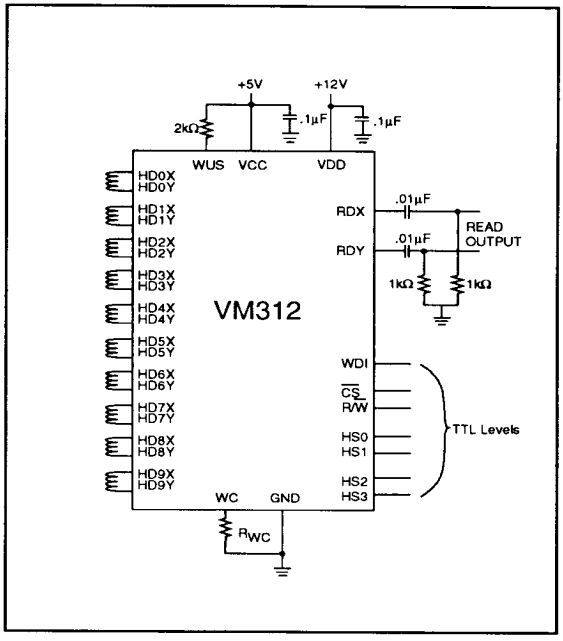
Table 1: Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Table 2: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TYPICAL APPLICATION



PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
HS0-HS3	I*	Head Select: selects one of ten heads
$\overline{CS}$	I	Chip Select: a low level enables the device
R/$\overline{W}$	I*	Read/Write: a high level selects Read mode
WUS	O*	Write Unsafe: Open collector output, high level indicates an unsafe writing condition
WDI	I*	Write Data In: a negative transition toggles the direction of the head current
H0X - H9X H0Y - H9Y	I/O	X,Y Head Connections
RDX, RDY	O*	X,Y Read Data: differential read data output
WC	*	Write Current: used to set the magnitude of the write current
VCC	-	+5V Logic Circuit Supply
VDD	-	+12V
GND	-	Ground

* When more than one R/$\overline{W}$ device is used, these signals can be wire OR'ed

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DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VDD Supply Current	I_{DD}	Read Mode			31	mA
		Write Mode			30 + I_W	
		Idle Mode			12	
VCC Supply Current	I_{CC}	Read Mode			47	mA
		Write Mode			27	
		Idle Mode			4.0	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		500	670	mW
		Write Mode: I_W = 20mA		625	800	
		Idle Mode		105	180	
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	V_{IL} = 0.8V	-0.4			mA
Input High Current	I_{IH}	V_{IH} = 2.0V			100	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.5	V
VDD Fault Voltage	V_{DDF}		9.0		10.5	V
VCC Fault Voltage	V_{CCF}		3.5		4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, $0 < V_{CC} \leq 3.5V$ $0 < V_{DD} < 9V$	-200		+200	µA
		Read/Idle Mode, $0 < V_{CC} < 5.5V$ $0 < V_{DD} < 13.2V$	-200		+200	

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READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, C_L (RDX, RDY) < 20pF and R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300KHz	125		175	V/V
Bandwidth	BW	-1dB I Zs I < 5Ω V_{IN} = 1mVp-p @300KHz	25			MHz
		-3dB I Zs I < 5Ω V_{IN} = 1mVp-p @300KHz	45			
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.65	0.8	$nV/\sqrt{Hz}$
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		17	26	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz (25°C < T_A < 125°C)	500	1000		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = VCC + 100mVp-p @5MHz	54			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} 100mVp-p @5MHz on V_{CC}	54			dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz Selected Channels V_{IN} = 0mVp-p	45			dB
Output Offset Voltage	V_{OS}		-250		+250	mV
RDX,RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} -2.8	V_{CC} -2.3	V_{CC} -2.0	V
		Write Mode	V_{CC} -2.8	V_{CC} -2.3	V_{CC} -2.0	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			30	Ω
Output Current	I_O	AC Coupled Load, RDX to RDY	3.2			mA

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			1.65		V
Differential Head Voltage Swing	V_{DH}	I_W = 40mA	7			Vp-p
Unselected Head Current	I_{UH}				1	mA(pk)
Differential Output Capacitance	C_{OUT}				25	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
WDI Transition Frequency	f_{DATA}	WUS = LOW	1.7			MHz
Write Current Range	I_W	41.25Ω < R_{WC} < 165Ω	10		40	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 40mA	-8		+8	%

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SWITCHING CHARACTERISTICS (See Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Read to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz Read Signal envelope or to 90% decay of write current			0.6	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz Read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0, 1, 2, 3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz Read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Prop. Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			32	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle & 1ns rise/fall time, L_H = 0, R_H = 0			0.5	ns
Rise/Fall Time	t_r/t_f	10%-90% points, I_W = 20mA L_H = 0, R_H = 0			5	ns
Rise/Fall Time	t_r/t_f	10%-90% points, I_W = 20mA L_H = 600nH, R_H = 20Ω			9	ns

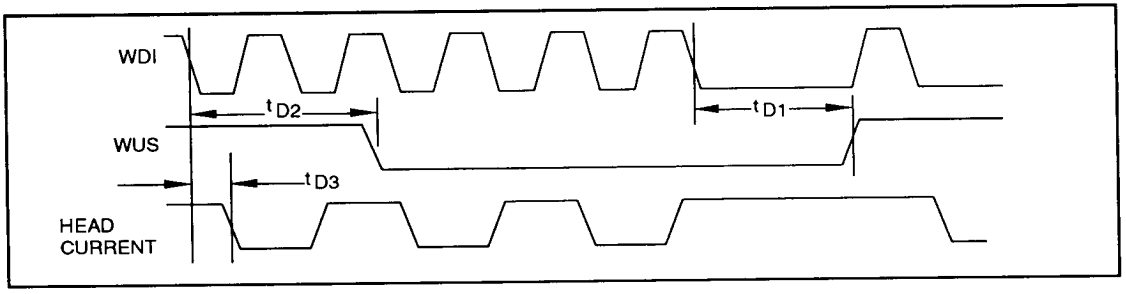

Figure 1: Write Mode Timing Diagram

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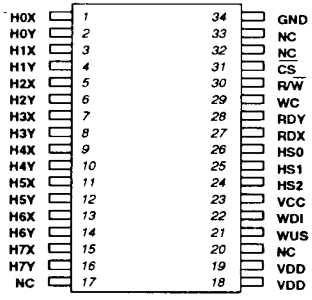
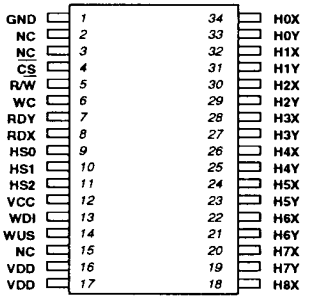
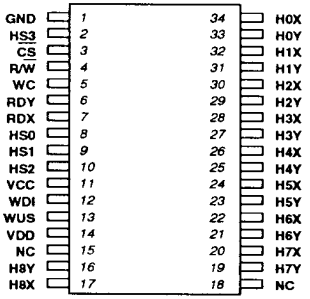
ADDITIONAL CONNECTION DIAGRAMS



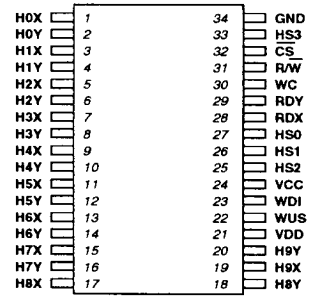
8-Channel
34-lead SOIC



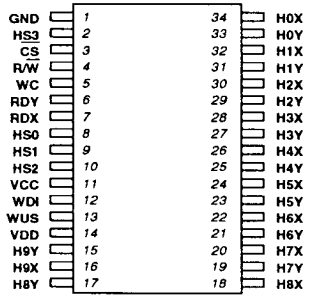
8-Channel
34-lead SOIC
(Mirror Version)



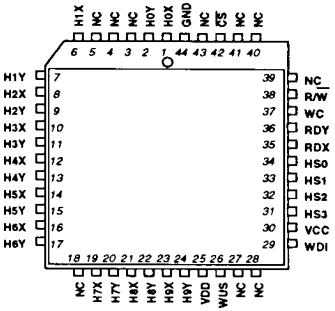
9-Channel
34-lead SOIC
(Mirror Version)



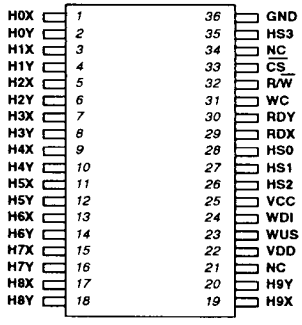
10-Channel
34-lead SOIC



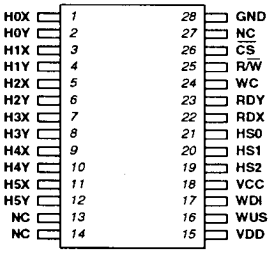
10-Channel
34-lead SOIC
(Mirror Version)



10-Channel
44-lead PLCC



10-Channel
36-lead SOIC



6-Channel
28-Lead SSOP

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